

FEC for High Speed Optical Transmission

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Abstract: This paper will at first explain the requirement of high speed optical transport network on forward error correction (FEC) codes in terms of code length, code rate, coding gain, burst error correction capability, error floor, latency, coding/decoding complexity. Then, a few code schemes used in current optical transport systems such as Reed-Solomon codes recommended by ITU-T G.709 and enhanced FECs listed in ITU-T, G.975.1 are introduced. Advanced codes recently developed by vendors used for 100Gbps systems and their performances are summarized. Features and special requirements on soft decoding FEC (SDFEC) especially inter-working between SDFEC and equalizer, with and without deferential coding etc. are analyzed. Some perspectives of future FEC for optical transport are also given.

1. General requirements on FEC

Net Coding Gain

As transport network usually covers long-haul and even ultra-long-haul transmission links. To reach the so called error-free (BER down to 10^{-12} or even 10^{-15}) transmission, FEC is an unavoidable technique. For the earlier stage Optical Transport Unit (OTU 0/1/2, with data-rate 1Gbps/ 2.5Gbps/10Gbps), Reed-Solomon (255,239) code was standardized by ITU-T G.709 [1], which has a net coding gain (NCG) at BER= 10^{-12} of 5.6dB. For Later OTU2/3 with data-rate 10Gbps/40Gbps ITU-T G975.1 recommended enhanced FECs containing 8 codes which have NCG@ 10^{-12} from 7.1dB to 9.0dB [2]. For 40Gbps and 100Gbps the vendors developed their own FEC with hard or soft decoding techniques which have better NCG (from 10dB to more than 11dB, ref. Fig. 4).

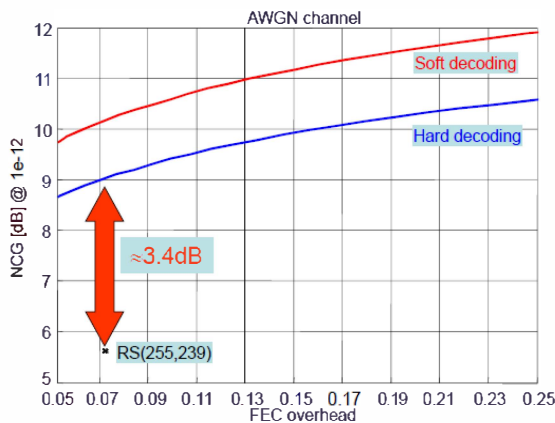


Fig. 1 Theoretical NCG bonds for AWGN channel

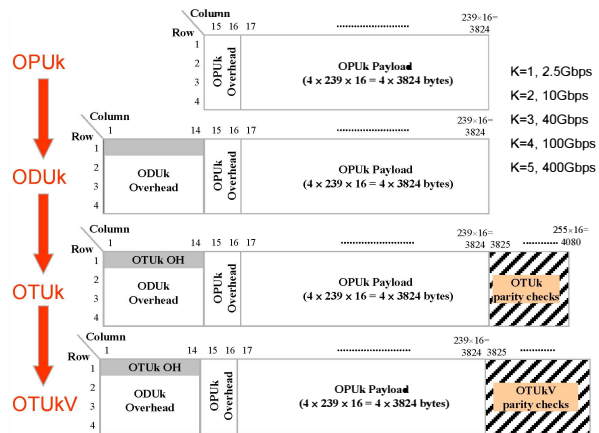


Fig. 2 OUT frame structure and FEC overhead

Latency

In addition to the NCG, also required is the coding/decoding latency, especially for delay-sensitive services such as financial data. The latency is resulted from coding/decoding process, buffering for interleaving and de-interleaving process. Usually the longer the code length is, the deeper the interleaver is, the more the latency will be.

Over Head

Theoretically the more overhead (OH) is spent for parity-check, the more NCG one will get. For 10G and below 10G system, usually 7% OH is applied. But for 100G and beyond system higher NCG is needed, codes with higher OH are investigated and applied. On the other hand, more OH means wider bandwidth of the coded signal. For

100Gbps PDM-QPSK systems, this is critical while its original signal bandwidth already fully occupies the 50GHz channel spacing. 100Gbps signals with FEC OH have to be narrow-filtered during transmission. One has to make trade-off between FEC's NCG and penalties resulted from narrow filtering effect and inter-channel cross-talk. Currently FEC OH for 100G systems are below 25%.

Code Length

According to coding theory, with the same OH longer codes have better NCG. But longer codes mean larger coding/decoding latency and more complex decoding. Another issue is that the code frame should match the OTN frame, so that both OTN frame and code frame have the common frame synchronization.

Complexity

To make the decoder realizable in ASIC, the decoding complexity should always be kept in mind of code designer. For hard decision FEC, its encoder/decoder can be a separate ASIC to the ASIC for coherent digital signal processing (DSP). As the advance of semiconductor technology, long codes with soft decoding are implementable into a CMOS ASIC. Nevertheless, the soft decoder has to be integrated with DSP into one ASIC because of wiring between these two modules. The FEC designers have to take this into account.

2. FEC for 100Gbps systems

For the earlier stage 100G transponder, if hard decoding FEC is used, FEC chip is usually mounted on the OUT board together with OUT framer/mapper. As soft decoding FEC is applied, it is hard to put FEC chip separate with the DSP chip because the high speed wiring is increased by 3-4 fold, depending on the quantization of the soft-information.

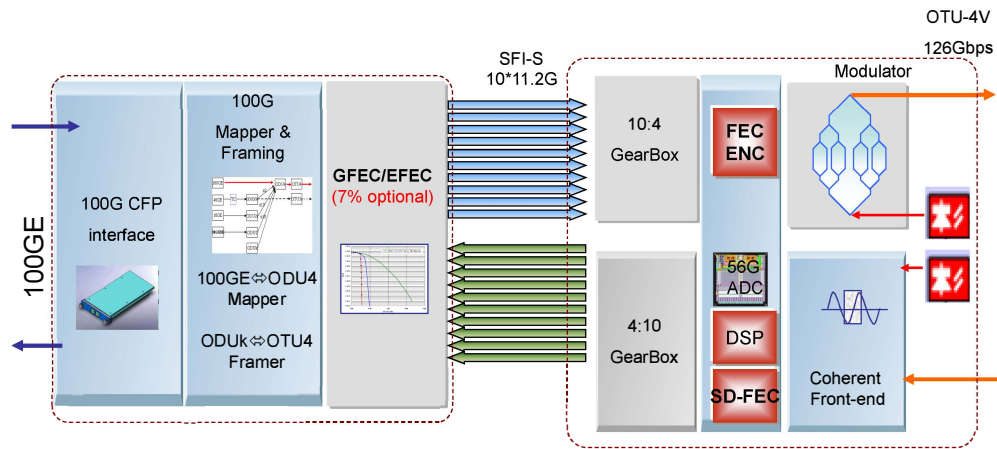


Fig. 3 FEC in 100G transponder

Apart from the codes recommended by ITU-T G.975.1, system vendors developed their own codes for 40G/100G coherent transmission systems.

Mitsubishi published the concatenated code with inner code of 13% LDPC and outer code of 7%RS code [3]. The LDPC code uses 2-bit soft decoding integrated with DSP together. RS code uses normal hard decoder. As the LDPC is relatively short, it suffers an error floor above 10^{-15} , RS code will push the error flow down below 10^{-15} . The total NCG reached 9.0dB.

Vitesse demonstrated both 7% and 20% Continuous- Interleaved BCH (CI-BCH) code both with hard decoding [4]. The 7%OH code reached an NCG of 9.3dB and the 20%OH code reached an NCG of 10.5dB.

ViaSat developed 7%OH hard decoding Turbo Product Code (TPC), 15%OH and 20%OH soft decoding TPC, which reach NCG of 9.3dB , 10.8dB and 11.3dB respectively [5].

Huawei published its 20%OH soft decoding LDPC code, which reaches NCG of 11.3dB [6].

3. Differential decoding and SD FEC

One critical issue of PDM-QPSK system is the phase cycle slip (phase jump of $\frac{\pi}{2}$ or multiples of $\frac{\pi}{2}$). It causes burst errors until the phase jumps back. If we use traditional FEC interleaving to diffuse these errors into different codes, it

does not remove these errors but converts them into random-like errors. This will degrade the error correction capability. One method to overcome the cycle slip is using differential coding (PDM-DQPSK). Differential decoding will convert the burst errors to be just one error at the burst beginning and one error at the burst end. On the other hand, differential decoding will convert one random error into two consecutive errors. Hard differential decoding DQPSK will result in 0.7dB penalty compared to QPSK without cycle slip at pre-FEC BER= 10^{-3} . If SD FEC is used, there is an issue about inter-working between differential decoder and soft FEC decoder. The differential decoder should work in soft-in soft-out mode. The simplest way is using soft differential decoding, namely multiplying current symbol with the conjugate of the previous symbol. As the multiplication almost doubles the additive noise power, this method will cause 2.7dB penalty compared to QPSK at pre-FEC BER= 10^{-3} . An improved method is applying log-likelihood ratio (LLR) calculation on the differential decoding logic and giving output LLR values to the soft FEC decoder. This approach will reduce the penalty down to 1.2dB [7]. A more advanced approach is to treat differential coding as a redundancy-free convolution code.

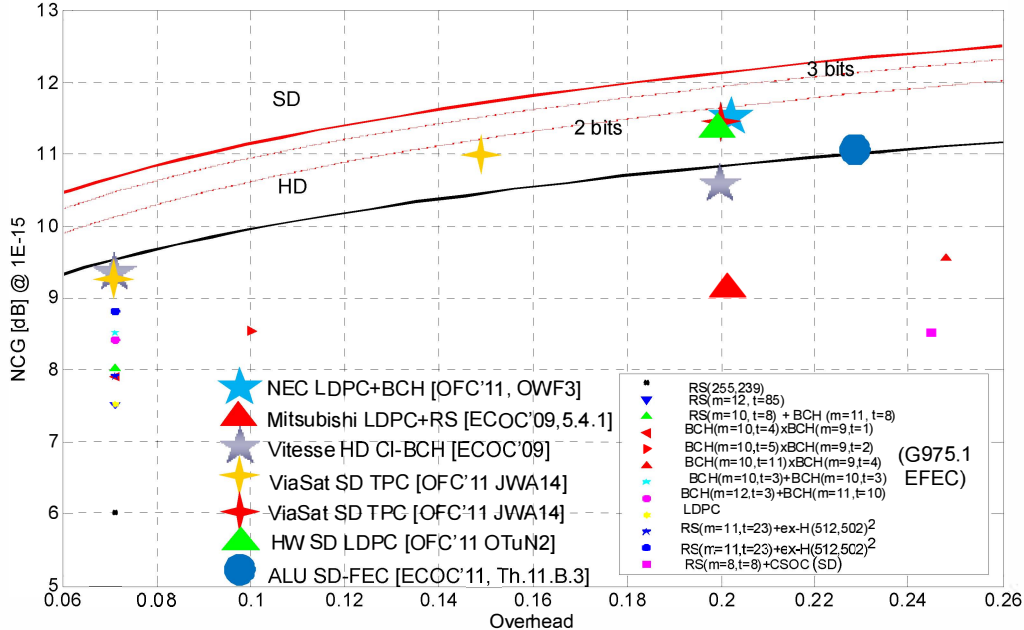


Fig. 4 NCG of G975.1 EFECs and recently published advanced FECs

One can use soft-in soft-out Viterbi algorithm for differential decoding. Furthermore iterative decoding between differential decoder and FEC decoder can be applied. This method will reduce the penalty down to 0.6dB with acceptable complexity [8]. Theoretically using this method the penalty can be completely eliminated depending on the FEC code structure.

4. Summary

In optical transport network, FEC is getting more and more important as transmission speed per GHz (usually called spectral efficiency) is increasing. As 100Gbps system is commercialized, there are some trends in the evolution of FEC, for example overhead is increased from 7% to 20% or even more; Decoding is moving from hard to soft. Vendors are developing their own advanced codes instead of using codes recommended by ITU-T. In research area, new codes such as convolutional LDPC codes, polar codes are introduced into optical communication. Joint coding and modulation, inter-working of coding and equalization, optimal decoding for non-AWGN optical channel, etc. are gaining more and more interest in the community.

References

- [1] Interfaces for the Optical Transport network, ITU-T G.709/Y.1331, 12/2009
- [2] Forward error correction for high bit-rate DWDM submarine systems, ITU-T G.975.1, 02/2004
- [3] T. Mizuoichi, et al., "FPGA based prototyping of next generation forward error correction", ECOC'09, 5.4.1
- [4] Vitesse Semiconductor, ECOC'09
- [5] S. Dave, et al., "Soft-decision forward error correction in a 40-nm ASIC for 100Gbps OTN applications", OFC'11 JWA14

- [6] D. Chang, et al., "FPGA verification of a single QC-LDPA code for 100Gb/s optical system without error floor down to BER of $1e-15$ ", OFC'11 OTuN2
- [7] A. Bisplinghoff, et al., "Soft decision metrics for differentially encoded QPSK", ECOC'11, Tu.6.A.2
- [8] F. Yu, et al., "Soft-decision LDPC turbo decoding for DQPSK modulation in coherent optical receivers", ECOC'11, We.10.P1.70